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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/982,335	10/18/2001	Nobuaki Tsuji	PW 027 7019 H7601US	6722

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Mr. Roger R. Wise
PILLSBURY MADISON & SUTRO LLP
Suite 1200
725 South Figueroa Street
Los Angeles, CA 90017

EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	09/982,335	TSUJI ET AL.	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

P ri d f r R ply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5,6,9,10,12,14-19,23-26 and 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6,9,10,12,14-19 and 23-26* is/are rejected.

7)☒ Claim(s) *27 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Pri rity under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 14 and 28 are objected to because of the following informalities:

The term "firs", as recited in claim 14, should read "first".

The phrase "equal to the second well region", as recited in claim 28, should read "equal to the depth of the second well region". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> **(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.**

Claims 9 and 15-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Groeseneken et al. (6,570,226).

Groeseneken et al. teach in figure 5 and related text a semiconductor input protection circuit comprising: a semiconductor substrate; a first active region 51 of a first conductivity type defined in the semiconductor substrate; a second active region (the region to the right of first active region 51) of a second conductivity type defined in the semiconductor substrate; first and second impurity doped regions 541, 542 of the

second conductivity type formed in the first active region; third and fourth impurity doped regions 551, 552 of the first conductivity type formed in the second active region; an input terminal 57 connected to the first impurity doped region 541; a first wiring for connecting the first active region 51 and the second impurity doped region 542 to the third impurity doped region 551; and a second wiring for connecting only the second active region and the fourth impurity doped region 552 to a reference potential 58. The first wiring is used for connecting the first active region 51 to the third impurity doped region 551 via the second impurity doped region 542. Note that the broad recitation of the claim does not require the first wiring to be used for directly connecting the first active region 51 to the third impurity doped region 551.

Regarding claim 15, Groeseneken et al. teach in figure 5 a first contact region 53 of the first conductivity type having a high impurity concentration, and formed in the first active region outside the first and second impurity doped regions, wherein the first wiring is connected via the first contact region 53 to the first active region 51.

Regarding claim 17, Groeseneken et al. teach in figure 5 a second contact region 58 of the second conductivity type having a high impurity concentration, and formed in the second active region outside the third and fourth impurity doped regions, wherein the second wiring is connected via the second contact region 56 to the second active region.

Regarding claims 16 and 18, Groeseneken et al. teach in figure 5 a first contact region and the third and fourth impurity doped regions and a second contact region and the first and second impurity doped regions having substantially the same impurity concentration and depth, respectively.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

1. Claims 1, 5, 23-26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (6,281,527) in view of Applicant Admitted Prior Art (AAPA). Chen teaches in figure 3 and related text an input protection circuit comprising: a semiconductor substrate 30 of a first conductivity type; a first well region 31 of a second conductivity type opposite to the first conductivity type, the first well region being formed in one principal surface area of the semiconductor substrate and forming a PN junction with the semiconductor substrate; first and second impurity doped regions 33, 32 of the first conductivity type formed in the first well region and forming a first lateral bipolar transistor with a portion of the first well region serving as a base; a second well region 40 of the first conductivity type formed in the principal surface area of the semiconductor

substrate; third and fourth regions 36, 34 of the second conductivity type formed in the second well region and forming a second lateral bipolar transistor with a portion of the second well region serving as a base, bottoms of the third and fourth well regions forming a PN junction with the second well or with the semiconductor substrate, an input terminal 1 formed on the semiconductor substrate; a circuit formed in the semiconductor substrate, and connected to the input terminal; and a reference potential node Vss formed on the semiconductor substrate; wherein the first and second lateral bipolar transistors are connected in series between the input terminal and the reference potential node, wherein the input terminal is connected to the first impurity doped region, the second impurity doped region and the base of the first lateral bipolar transistor are connected to the third well region (the second impurity doped region is electrically connected to the third well region via N-well 31), the first lateral bipolar transistor operating without a fixed base bias, and the fourth well region and the base of the second lateral bipolar transistor are connected to the reference potential node.
Chen does not teach third and fourth regions being third and fourth well regions.
AAPA teaches in figure 10 third and fourth regions 5, 6 being formed as third and fourth well regions 3, 4.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the third and fourth regions in third and fourth well regions in Chen's device, in order to provide high inverse breakdown voltage to the protection device.

Regarding claim 5, a portion of the semiconductor substrate serves as a base in Chen's device, because the P type substrate and the P well base region have the same conductivity type, thus rendering the substrate as being part of the base region.

Regarding claims 23-26, the claimed limitations of first and second lateral bipolar transistors being turned on to protect the input protection circuit when high positive or negative voltage are applied to the input terminal, are inherent in Chen's device, because Chen's structure is identical to the claimed structure.

Regarding claim 28, AAPA teaches third and fourth well regions having a depth almost equal to the depth of the second well region. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the third and fourth well regions to have a depth almost equal to the depth of the second well region in Chen's device, in order to provide high inverse breakdown voltage to the protection device.

2. Claims 5, 10, 12, 19 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Groeseneken et al. (6,570,226) in view of Applicant Admitted Prior Art (AAPA).

Groeseneken et al. teach in figure 5 and related text an input protection circuit comprising: a semiconductor substrate of a first conductivity type; a first well region 51 of a second conductivity type opposite to the first conductivity type, the first well region

being formed in one principal surface area of the semiconductor substrate and forming a PN junction with the semiconductor substrate; first and second impurity doped regions 541, 542 of the first conductivity type formed in the first well region and forming a first lateral bipolar transistor with a portion of the first well region serving as a base;

Second and third regions 551, 552 of the second conductivity type formed in the semiconductor substrate and forming a second lateral bipolar transistor with a portion of the semiconductor substrate serving as a base; a circuit formed in the semiconductor substrate, and connected to the input terminal; and a reference potential node Vss formed on the semiconductor substrate; wherein the first and second lateral bipolar transistors are connected in series between the input terminal and the reference potential node, wherein the input terminal is connected to the first impurity doped region, the second impurity doped region and the base of the first lateral bipolar transistor are connected to the third well region, the first lateral bipolar transistor operating without a fixed base bias, and the third region and the base of the second lateral bipolar transistor are connected to the reference potential node.

Note that the broad recitation of the claim does not require the base of the first lateral bipolar transistor to be directly connected to the third well region.

Groeseneken et al. do not teach second and third regions being second and third regions.

AAPA teaches in figure 10 second and third regions 5, 6 being formed in second and third well regions 3, 4.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the second and third regions as second and third well regions in Groeseneken et al.'s device, in order to provide high inverse breakdown voltage to the protection device.

Regarding claim 10, Groeseneken et al. teach substantially the entire claimed structure, as applied to claim 9 above, except third and fourth impurity doped well regions reaching a bottom of the second active region. AAPA teaches in figure 10 the third and fourth impurity doped well regions 3, 4 reach a bottom of the second active region. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the third and fourth regions to reach a bottom of the second active region in Groeseneken et al.'s device, in order to provide high inverse breakdown voltage to the protection device.

Regarding claim 19, Groeseneken et al. and AAPA teach a first contact region 53 (Groeseneken et al., figure 5) of the first conductivity type having a high impurity concentration, and formed in the first active region outside the first and second impurity doped regions, wherein the third and fourth impurity doped regions each include a surface side high impurity concentration region and a deeper low impurity concentration region, and have substantially the same impurity concentration and depth as the surface side high impurity concentration region and the first contact region.

Regarding claims 25-26, the claimed limitations of first and second lateral bipolar transistors being turned on to protect the input protection circuit when high positive or negative voltage are applied to the input terminal, are inherent in Groeseneken et al.'s device, because Groeseneken et al.'s structure is identical to the claimed structure.

3. Claims 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen and AAPA, as applied to claims 1 and 5 above, and further in view of Watt (5,477,413).

Regarding claims 2 and 6, Chen and AAPA teach substantially the entire claimed structure, as applied to claims 1 and 5 above, including a current limiting resistor R1 (Chen, figure 4) formed on a principal surface area of the semiconductor substrate, wherein the input terminal is connected via the current limiting resistor to the first impurity doped region, and an insulating layer 8 (AAPA, figure 10) formed in the principal surface area of the semiconductor substrate. Chen and AAPA do not explicitly state forming the resistor on the semiconductor substrate.

Watt teaches in figure 5 forming resistor 58 on the semiconductor substrate (column 7, lines 29-35). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the resistor on the semiconductor substrate in Chen and AAPA's device, in order to provide better control over the resistance value and thus the characteristics of the device.

4. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Groeseneken et al. and AAPA, as applied to claims 5 and 9 above, and further in view of Watt (5,477,413).

Regarding claim 6, Groeseneken et al. and AAPA teach substantially the entire claimed structure, as applied to claim 5 above, including a current limiting resistor R1 (Groeseneken et al., figure 6) formed on a principal surface area of the semiconductor substrate, wherein the input terminal is connected via the current limiting resistor to the first impurity doped region, and an insulating layer 8 (AAPA, figure 10) formed in the principal surface area of the semiconductor substrate. Groeseneken et al. and AAPA do not explicitly state forming the resistor on the semiconductor substrate.

Watt teaches in figure 5 forming resistor 58 on the semiconductor substrate (column 7, lines 29-35). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the resistor on the semiconductor substrate in Groeseneken et al. and AAPA's device, in order to provide better control over the resistance value and thus the characteristics of the device.

Allowable Subject Matter

Claims 27 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

R asons for allowanc

The following is an examiner's statement of reasons for allowance:

Chen (6,281,527) and Applicant Admitted Prior Art (AAPA) appear to be the closest prior art reference. Chen and AAPA teach substantially the entire claimed structure as recited in claim 1, except a third well region being formed entirely inside the second well region, as recited in claim 27, and third and fourth well regions not being part of a MOS transistor, as recited in claim 29. Therefore, prior art do not teach or render obviousness the semiconductor structure, as claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

5. Applicant argues on page 12 that Chen does not disclose third and fourth regions 34 and 36 form a second lateral bipolar transistor.

Although Chen does not explicitly state that third and fourth regions 34 and 36 form a second lateral bipolar transistor, PNP junctions are formed between third region 34, P-well 40 and fourth region 36, thus forming a second lateral bipolar transistor, even if the second lateral bipolar transistor may be only a parasitic bipolar transistor.

6. Applicant argues on page 13 that Chen does not disclose a second impurity doped region being connected to the third well region.

Chen teaches a second impurity doped region being electrically connected to the third well region via N-well 31. The broad recitation of the claim does not require the second impurity doped region to be directly connected to the third well region.

7. Applicant argues on pages 13-15 and 21-23 that AAPA does not teach the claimed invention, and placing the AAPA'S circuit into the Chen and Groeseneken et al references would destroy the purpose of the Chen reference because of the different electrical connections to the drain, gate, and source of the MOS transistor that are present in the AAPA.

One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Chen and Groeseneken et al. teach substantially the entire claimed structure, whereas AAPA is only cited to teach an artisan that it is obvious to form impurity regions as well regions.

8. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning for combining AAPA with Chen and Groeseneken et al., it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long

as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

9. Applicant argues on page 20 that Groeseneken et al. do not disclose an N well 51 being connected to the second well region 551.

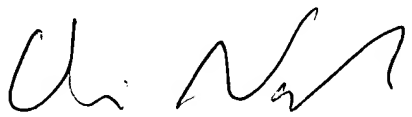
Groeseneken et al. teach an N well 51 being electrically connected to the second well region 551 via PN junction 542. The broad recitation of the claim does not require N well 51 to be directly connected to the second well region 551.

10. The rest of applicant's arguments with respect to claims 9-10, 12 and 14-19 have been considered but are moot in view of the new ground(s) of rejection.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applicati ns.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**



O.N.
February 9, 2004

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800